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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,760	11/17/2003	Paul Evans	858063.458C1	3370

38106 7590 05/27/2004

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EXAMINER	
NGUYEN, THINH T.	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,760	EVANS, PAUL	
	Examiner	Art Unit	
	Thinh T Nguyen	2818	

-- Th MAILING DATE of this communication appears on the cov r sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/085,121.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Claims 1-28 are pending in the Application.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claims Objections

3. Claim 6 is objected to for the following informalities:

in claim 6 line 3 " a stack of modules " should be -- the stack of module --.

Correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 1-3,6-8,10-14,16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Khosrowpour et al. (U.S. Patent 6,477,593).

REGARDING CLAIM 1

Khosrowpour et al. (fig. 1 reference numeral 100, column 4 line 9-10) disclose a stackable module for a processor system, the module comprising: a support plate (fig 1 reference numeral 120,130,column 4 line 12) having a topside and an underside; a set of topside circuit components (fig 1) mounted on the topside of the support plate, the circuit components constituting a transport stream generating device that generates transport stream data and transport stream control signals; a topside connector(fig 2 reference numeral 122A,122B) mounted to the topside of the support plate; an underside connector mounted to the underside of the support plate(fig 2 reference numeral 122C,122D) ; and a first set of conductive tracks (fig 2 reference numeral 114A,114B) connected directly between the topside connector and the underside connector and a second set of conductive tracks connecting the topside connector to the set of topside circuit components, the underside connector and the topside connector being engageable with respective underside connectors and topside connectors of other modules, the first and second set of conductive tracks arranged to convey the transport stream data and the transport stream control signals in a stack of modules.

REGARDING CLAIM 2

Khosrowpour et al. (fig. 1-4) disclose a stackable module wherein each of the topside and underside connectors comprises a set of pins for carrying memory access signals to enable the module to function as an external memory interface.

REGARDING CLAIM 3

Khosrowpour et al. (fig. 1) disclose a stackable module wherein the topside connector is a receptacle and the underside connector is a plug

REGARDING CLAIM 6

Khosrowpour et al.(fig. 2) disclose a stackable module comprising a connector space defining a component that extends from the support plate by a distance calculated to define the minimum spacing in a stack of modules.

REGARDING CLAIM 7,8,12,13,14

Khosrowpour et al.(the abstract, fig 1-4) disclose a stackable module that has top side circuit's components 134, 124 that can function as multiplexor (switching function) or transport stream generating device that generate transport stream data and transport stream control signal.

REGARDING CLAIM 10

Khosrowpour et al. (the abstract, fig 1-4) disclose a stack of modules in a processor system, the stack comprising: a main board having an interface connector and a set of main board components, the interface connector providing a set of pins for conveying transport stream data and transport stream control signals; at least one module comprising a support plate with an underside connector mounted to an underside of the support plate and a topside connector mounted to a topside of the support plate, the at least one module comprising a transport stream generating device configured to generate the transport stream data and the transport stream control signals, the underside connector being connected to the interface connector of the main board for conveying the transport stream data and the transport stream control signals from the at least one module to the interface connector of the main board.

REGARDING CLAIM 11

Khosrowpour et al. (the abstract, fig 1-4) disclose a stack of modules in a processor system, the stack comprising: a main board (fig 1 reference 110) having an interface connector and a set of main board components, the interface connector providing a set of pins for conveying transport stream data and transport stream control signals; at least one module comprising: a support plate having a topside and an underside; a set of topside circuit components mounted on the topside of the support plate and comprising a transport stream generating device configured to generate the transport stream data and the transport stream control signals; a topside connector mounted to the topside of the support plate; an underside connector mounted to the underside of the support plate and connected to the interface connector of the main board; and a first set of conductive tracks connected directly between the topside connector and the underside connector and a second set of conductive tracks connecting the topside connector to the topside circuit components, the underside connector and the topside connector being engaged with respective underside connectors and topside connectors of other modules in the stack, the first and second set of conductive tracks arranged to convey the transport stream data and the transport stream control signals in the stack of modules.

REGARDING CLAIM 16

Khosrowpour et al. (the abstract, fig 1-4) disclose a stack of modules in a processor system, the stack comprising: a main board (fig 1 reference 110) having an interface connector and a set of main board components, the interface connector providing a set of pins for conveying transport stream data and transport stream control signals; and a plurality of modules, each module comprising a support plate with an underside connector mounted to an underside of

the support plate and a topside connector mounted to a topside of the support plate, each module comprising a transport stream generating device configured to generate the transport stream data and the transport stream control signals, the underside connector of a lower one of the modules connected to the interface connector of the main board for conveying the transport stream data and the transport stream control signals from the lower module to the interface connector of the main board.

REGARDING CLAIM 17

Khosrowpour et al. (the abstract, fig 1-4) disclose a stackable module for a processor system, the module comprising: a support plate having a topside and an underside; a set of topside circuit components mounted on the topside of the support plate, the circuit components constitute a device which acts on transport stream data and transport stream control signals; a topside connector mounted to the topside of the support plate; an underside connector mounted to the underside of the support plate; a first set of conductive tracks (122A,122B) connected directly between the topside connector and the underside connector and a second set of conductive tracks(122C,122D) connecting the topside connector to the topside circuit components, the underside connector and the topside connector being engageable with respective underside connectors and topside connectors of other modules, the conductive tracks arranged to convey the transport stream data and the transport stream control signals in a stack of modules; and a multiplexor for selectively selecting the transport stream data from a lower module in the stack and an upper module in the stack for acting on by the device.

6. Claim 9,15, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Jasper (US patent 6,109,929).

REGARDING CLAIM 9,15

Jasper discloses (fig 4A,fig 4B,fig 7, component 27 ,column 6 line 32-35 , lines 47-59) a stackable module for a processor system wherein the circuit component comprises a device that does not utilize the transport stream data and the transport stream control signals, said transport stream data and control signals supplied via said topside and underside connectors directly to another module in a stack of modules.

REGARDING CLAIM 18

Jasper discloses (fig 4A,fig 4B,fig 7, component 27 ,column 6 line 32-35 , lines 47-59) a stackable module for a processor system, the module comprising: a support plate having a topside and an underside; a set of topside circuit components mounted on the topside of the support plate; a topside connector mounted to the topside of the support plate; an underside connector mounted to the underside of the support plate; and a first set of conductive tracks connected directly between the topside connector and the underside connector and a second set of conductive tracks connecting the topside connector to the topside circuit components, the underside connector and the topside connector being engageable with respective underside connectors and topside connectors of other modules, the conductive tracks arranged to convey transport stream data and transport stream control signals between modules in a stack of modules; and wherein the circuit components constitute a device that does not utilize the transport stream data and the transport stream control signals, all of the transport stream data and

the transport stream control signals being supplied via said topside and underside connectors directly to another module in the stack of modules.

7. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Brekosky et al. (US patent 6,431,879).

REGARDING CLAIM 19

Brekosky et al.(in fig. 1, fig 2, fig 3) disclosed a stackable printed circuit board (PCB) configured for stacking on a motherboard and with other stackable printed circuit boards (PCBs) in combination, comprising: at least one support pillar (fig 1 reference 15,16) extending from a top surface of a PCB; and at least one through-hole formed in the PCB and adapted to receive a support pillar from another stackable PCB.

Claim Rejections - 35 USC § 103

8. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 20-22,24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al. (U.S. patent 6,477,592) in view of further remark.

REGARDING CLAIM 20

Khosrowpour et al. (fig 1-fig 4) disclose all the invention except for the teachings of making one through hole for receiving a support pillar. This feature, however, is considered obvious since it is old and well known in the art.

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings of Khosrowpour et al. with his regular routine design skill in order to come up with the invention of claim 20 .

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to make a provision for a hole for support pillar for the purpose of improving its mechanical strength as it is well known in the art that the support pillar or spacers increase the strength of a stacked PCB assembly against stress.

REGARDING CLAIM 21

Khosrowpour et al. (fig. 1-4) disclose a stackable module wherein each of the topside and underside connectors comprises a set of pins for carrying memory access signals to enable the module to function as an external memory interface.

The rationale why claim 21 is obvious over Khosrowpour et al. has been discussed in the rejection of claim 20.

REGARDING CLAIM 22

Khosrowpour et al. (fig. 1) disclose a stackable module wherein the topside connector is a receptacle and the underside connector is a plug.

The rationale why claim 22 is obvious over Khosrowpour et al. has been discussed in the rejection of claim 20.

REGARDING CLAIM 24

Khosrowpour et al.(fig. 2) disclose a stackable module comprising a connector space defining a component that extends from the support plate by a distance calculated to define the minimum spacing in a stack of modules.

The rationale why claim 24 is obvious over Khosrowpour et al. has been discussed in the rejection of claim 20.

REGARDING CLAIM 25,26,27

Khosrowpour et al.(the abstract, fig 1-4) disclose a stackable module that has top side circuits components 134, 124 that can function as multiplexor (switching function)or act on (to process) transport stream data or transport stream control signal or generate transport stream data and transport stream control signal.

The rationale why claim 25,26,27 are obvious over Khosrowpour et al. has been discussed in the rejection of claim 20.

10. Claim 4, 28 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Jasper (US patent 6,109,929) in view of further remark.

REGARDING CLAIM 4, 28

Jasper (fig 4A,fig 4B,fig 7, component 27 ,column 6 line 32-35 , lines 47-59) discloses all the invention including a device (component 27) that does not utilize the transport stream data and the transport stream control signals, said transport stream data and control signals being

supplied via said topside and underside connectors directly to another module in a stack of modules. Missing in the teachings of Jasper is the incorporation of a through hole

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings of Khosrowpour et al. with his regular routine design skill in order to come up with the invention of claim 28 .

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to make a provision for a hole for support pillar for the purpose of improving its mechanical strength as it is well known in the art that the support pillar or spacers increase the strength of a stacked PCB assembly against stress.

11. Claims 5, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khosrowpour et al. (US patent 6,477,593) in view of Brekosky et al. (US patent 6,431,879).

REGARDING CLAIM 5, 23

Khosrowpour et al. (the abstract, fig 1-4) disclose all the invention except for a support pillar. Brekosky et al., however, (in fig. 3, column 2 lines 21-32) teach how to built a support pillar.

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings by Khosrowpour et al. with the teachings by Brekosky et al. in order to come up with the invention of claim 5 or 23

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to make a provision for support pillar for the purpose of improving its mechanical strength as it is well known in the art that the support pillar or spacers increase the strength of a stacked PCB assembly against stress and moreover, a person skilled in the art would like to make a system easier to assemble as suggested by Brekosky et al (column 1 lines 42-43).

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1-28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-15 of U.S. Patent 6,731,514 . Although the conflicting claims are not identical, they are not patentably distinct from each other. Claims 1-28 of the present invention is a similar version of the claimed invention in claims 1-15 of the above-identified U.S. Patents with similar intended scope. A person skilled in the art at the time the invention was made would be able to use the information of claims 1-15 of US patent 6,731,514 and his routine design skill in order to come up with inventions of claims 1-28 of the present application.

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

15. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

16. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) in parent Application 10/ 085,121 which papers have been placed of record in the file.

CONCLUSION

17. The prior arts made of record and not relied upon are considered pertinent to applicant disclosure: Chang (US patent 6,552,914) disclose a circuit board assembly mechanism.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thinh T. Nguyen TTN

Art Unit 2818

David Nelms
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